
INDEX

INDEX

SUBJECTS

A

- Abdominal imaging, ultrasound, II.32
- Absolute value circuit, II.4, 15-16
 - op-amp, II.4
- AC linearity plot, III.25-26
- Active filter, III.37
- AD7528 Dual 8-Bit CMOS DAC Application Note, II.51
- Adams, R.W., VI.30
- Adaptive pulse code modulation system, See: ADPCM
- ADC, I.2, 6, II.20, 31-2, 34, 36, 39, III.3, 7-9, 25, 27, VII.1-2, 22
 - 3-bit,
 - ideal, analog input, III.18
 - non-ideal, analog input, III.18
 - 8-bit, subranging, IV.5
 - 12-bit, subranging, IV.6
 - 14-bit, recursive, IV.7
- AC linearity, III.26
- aperture delay time, III.27
- aperture jitter, III.27-28
- best-fit sinewave, III.15
- busy/interrupt, IX.4
- conversion complete, IX.4
- converter encoder, IV.2
- data acquisition, III.29
- data ready, IX.4
- data valid, IX.4
- DCS, IV.5-6
- demodulation, III.10-11
- digital output, III.17
- DMA, IX.4
- DMD, IX.4
- DNL, III.17
- DNL plot, III.25-26
- DSP applications, IV.1
- DSP interface, IX.14
- dual slope, IV.8
- dynamic performance, III.21
- dynamic range, III.12
- dynamic specifications, III.21
- dynamic testing, III.14
- effective aperture delay time, III.27
- encode command, IX.4
- end-of-conversion, IX.4
- ENOBs, III.15, 21
- errors, III.18
- FFT output, III.14
- finite amplitude resolution, III.12
- flash, IV.3-4
 - N-bit, IV.3
 - performance, III.22
- FLB, III.23
- FPBW, III.23-24
- gain error, III.17
- ground, XI.37
- and harmonic distortion, III.17
- IMD, III.25
- INL, III.17
- input, ripple, IV.9
- integrator, IV.8
 - charge/discharge, IV.8-9
 - hysteresis and offset, IV.9
 - leakage and offset, IV.9
 - normal mode, IV.9-10
 - sampling period, IV.9
- interfacing, IX.1
- intermodulation, III.24
- memory-mapped, IX.1
- missing codes, III.17
- offset error, III.17
- overvoltage recovery, III.30
- parallel, to DSP, IX.4
- parallel interface, IX.4
- peak spurious response, III.23
- quantization noise, III.5, 12
- read data, IX.4
- recursive subranging, IV.7

- resolution and dynamic range, III.12, 16
- S/N+D, III.15, 21
- sampling, III.21-22, IV.4
- sampling converter, IV.1
- SAR with SHA, IV.1-3
- serial, to DSP, IX.15
- serial interface timing, IX.18
- serial output, IX.17
- settling time, III.29
- SHA, III.24
- sigma-delta technology, IV.9
- sinewave, III.15
- SNR, III.12, 21
 - aperture jitter, III.28
- start-convert, IX.4
- state of the art, I.7
- static performance specifications, III.17
- static transfer characteristics, III.17
- subranging, IV.5
 - 8-bit, IV.5
 - 12-bit, IV.6
 - digital correction, IV.5
- successive approximation, IV.1-2
- testing, III.13
- THD, III.23
- theoretical RMS error, III.15-16
- transfer function, III.18
- transient response, III.29
- tri-state output, IX.26
- ADC/ADSP, IX.2
- ADC/ADSP-2100, parallel interface, IX.7
- ADC/ADSP-2101:
 - parallel interface, IX.4
 - DMACK, IX.6
 - parallel read interface, timing, IX.5
- ADC/TMS32020/C25, parallel interface, IX.7
- Adder:
 - instrumentation amp, II.2
 - op-amp, II.2
- ADDS-2101-SW DSP Software Development Tools, Data Sheet, VIII.19
- ADPCM, I.3
- ADSP-2100, drive capability, XI.53
- ADSP-2100 Family Applications Handbook, VIII.19
- ADSP-2100 Family Applications Handbook Vol. 4, X.30
- ADSP-2100 User's Manual/Architecture, IX.28
- ADSP-2100/2102 User's Manual/Architecture, IX.28
- ADSP-2100/ADSP-2100A Digital Signal Processor, Data Sheet, VIII.19
- ADSP-2100A, wait state generation, IX.29-32
- ADSP-2101:
 - with ADC, DAC, and DSP, IX.1
 - DMA, IX.4
 - DMS, IX.4
 - I/O port interface, IX.24
 - memory write timing, IX.9
 - memory-mapped peripherals, IX.26
 - output enable, IX.3
 - parallel interface, IX.2
 - parallel read timing, IX.3
 - parallel write timing, IX.10
 - in QAM, X.6
 - RD, IX.4
 - RD timing, IX.2
 - serial interface, IX.17, 22
 - serial port, IX.15
 - serial port interface, IX.26
 - serial port receive timing, IX.16
 - serial port transmit timing, IX.20
 - V.32 modem,
 - program memory, X.8
 - serial interface, X.9-10
 - wait state generation, IX.29-32
- ADSP-2101 Cross-Software Manual, VIII.19
- ADSP-2101 DSP Microcomputer, Data Sheet, VIII.19
- ADSP-2101 Emulator, Data Sheet, VIII.19
- ADSP-2101 Emulator Manual, VIII.19
- ADSP-2101 EZ-ICE Manual, VIII.19
- ADSP-2101 EZ-LAB Manual, VIII.19
- ADSP-2101 microcomputer, VIII.9
 - architecture, VIII.5-6
 - configuration, VIII.17

- DAG, VIII.6
- development system, VIII.18
- DMA bus, VIII.7
- DMD bus, VIII.7
- PMA bus, VIII.7
- PMD bus, VIII.7
- program sequencer, VIII.15
- result bus, VIII.7
- serial ports, VIII.16
- shifter, VIII.11
- single-instruction cycle, VIII.5
- system interface, VIII.17
- ADSP-2101 User's Manual, VIII.19
- ADSP-2101-EZ Tools, Data Sheet, VIII.19
- ADSP-2105 DSP Microcomputer, Data Sheet, VIII.19
- ADSP-2111 DSP Microcomputer with Host Port, Data Sheet, VIII.19
- ADSP-2111 User's Manual, VIII.19
- ADSP-21msp50:
 - GSM benchmarks, X.18
 - mixed signal processor, X.17
 - optimized DSP, X.16
 - specifications, X.17
- ADSP-21XX DSP Hardware Development Tools, Data Sheet, VIII.19
- ADSP-21XX DSP Software Development Tools, Data Sheet, VIII.19
- ADSP-28msp01:
 - integrated modem, analog front end, X.10
 - specifications, X.10-11
- ADSP-28msp02 CODEC serial port DSP interface, IX.26
- ADSP-28msp02 sigma-delta CODEC, IX.25
- ADSP-28msp02 sigma-delta voiceband CODEC, IX.25
- AGC loop, in disk drive read amplifier, II.5
- AGND, XI.36-38
- AIN, IV.7
- Aliasing:
 - dynamic range of sample, III.3-5
 - frequency domain effect, III.4
 - on dynamic range, III.4
 - time domain effect, III.3
 - unwanted tones, III.5
- Allen, P.E., II.52
- ALU:
 - features, VIII.8-9
 - instructions, VIII.9
 - register, VIII.9
- Amplifier, signal conditioner, I.8
- Amplitude shift keying, See: ASK
- Analog beamforming, II.34
- Analog cellular radio:
 - FDMA, X.11-2
 - frequency reuse, X.11-12
 - frequency spectrum allocation, X.12
 - problems, X.11
 - TDMA, X.13
- Analog circuit:
 - ESD, XI.9
 - high frequency decoupling, XI.23
 - high frequency instability, XI.24
 - noise, XI.36-37
 - SPICE modeling, XI.58-59
- Analog computation, with multiplier, II.14
- Analog computer, II.21, 24
- Analog downconversion, III.10
- Analog filtering:
 - active, II.37-38
 - passive, II.37
- Analog ground, See: AGND
- Analog multiplexer, III.29
- Analog multiplier, II.8-9
 - logarithmic, II.9
- Analog signal:
 - aliasing, III.2-4
 - bandwidth, sampling, III.2
 - conditioning and processing, I.6
 - discrete sampling, III.2
 - moving average FIR, VII.5
 - routing, XI.44
- Analog signal processing, I.6, II.5
 - amplifier, II.1
 - filtering, II.37
 - mathematical operations, II.1
 - options, I.6
- Analog sound recording:

- additive noise, X.21
- degradation, X.21
- nonlinearities, X.21
- Analog-to-digital conversion, III.1
- Analog-to-digital converter, See: ADC
- Andreas, D., VI.30
- Andrews, James R., III.43
- Antialiasing filter, III.6, 42
 - alpha value, II.44-45
 - audio, II.49
 - design, II.44, III.7
 - FDNR, II.44-45, 47-49
 - FDNR audio, II.49
 - frequency value, II.44-45
 - multiple feedback, II.44-46
 - out-of-band attenuation, III.7
 - oversampling, III.7
 - requirements, III.6
 - Sallen-Key, II.44-46
 - See: Antialiasing filter
 - selection, III.5-6
 - simplification, III.8
 - specifications, II.44
 - state variable, II.44-45, 47-48
 - tuning, II.44-45
- Aperture delay time, III.27
- Aperture jitter, III.27-28
- Arithmetic logic unit, See: ALU
- Arithmetic status register, See: ASTAT
- ASK, modulation, X.3
- ASTAT, VIII.14
- Audio:
 - DAC,
 - glitch minimization, V.5
 - segmentation, V.6
- Audio filter, III.38
- Audio line driver, I.14
 - balanced, I.14
 - differential, I.14
 - high common-mode rejection, I.14
- Audio line receiver, I.15
 - differential, I.14
- Audio power meter, multiplier, II.13
- Automatic gain control, See: AGC

B

- Balanced audio line driver, I.14
- Balanced modulator, II.15-16
- Baldwin, Eugene E., III.43
- Barber, William L., II.51
- Barrow, Jeff, XI.63
- Basic diode log amp, II.21
- Basic multiplier, II.8
- Beamforming:
 - analog, II.35
 - digital, II.35
- Bell, Barry A., III.43
- Bennett, W.R., III.13, 43
- BiMOS current switch, V.4
- BiMOS DAC, V.4
- Binary current scaling, DAC, V.1
- Binary logic circuit:
 - logic states, XI.3
 - noise immunity, XI.3
- Bingham, John, X.30
- Blackman, R.B., III.43
- Bleaney, B., XI.63
- Bleaney, B.I., XI.63
- Blinchikoff, H.J., II.51
- Blood, signal attenuation, II.34
- BMS, DSP, parallel interface, IX.1
- Boot memory select, See: BMS
- Boser, B., VI.30
- Boyd, I., X.30
- Broadband Amplifier Applications, II.51
- Brodersen, Gray, III.44
- Brokaw, Paul, XI.63
- Brown, Edmund R., II.51
- Budak, A., II.51
- Buffer latch, as Faraday shield, XI.21
- Burton, Phil, V.19
- Butterfly calculation, VII.30
- Butterworth filter, II.39, VII.19
 - design, II.44
 - maximally flat filter, II.39

C

- Cable driver:
 - inverting, I.16
 - noninverting, I.16
- Calhoun, George, X.30
- Capacitance, XI.15
 - stray, XI.15-16
 - tuned circuit, XI.31
- Capacitive coupling equivalent circuit, XI.16
- Capacitive noise, XI.16
- Capacitive shield, XI.17
- Capacitor:
 - dielectric absorption, XI.24
 - electrolytic, leakage, XI.22
 - equivalent circuits, XI.21
 - inductance, XI.22
 - leakage, XI.22
 - parasitic effects, XI.21
 - series/loss resistance, XI.22
 - SHA,
 - dielectric absorption, XI.25
 - leakage, XI.22
- Cascaded gain stage, II.31-32
- Cascaded limiting amplifier, II.25
 - gain, II.26
 - response curve, II.26
- Cascaded semi-limiting amplifier, II.21, 25
- Caves, J.T., III.44
- CB processes, DAC, V.1-2
- CCITT, recommendations, X.3
- CD player:
 - 18-bit,
 - 8X oversampling,
 - 3-pole antialiasing filter, X.27-28
 - reconstruction electronics, X.26
 - 20-bit,
 - 8X oversampling,
 - reconstruction electronics, X.27
 - THD+N, X.28-28
- ADC, X.22
 - antialiasing filter, X.25
 - audio DAC, CD, X.28-29
 - design,
 - digital filtering effects, X.26
 - oversampling effects, X.26
 - first generation, reconstruction electronics, X.24
 - oversampling, SNR, X.25
 - read electronics, X.23-24
 - second generation,
 - 18-bit, 8X oversampling, X.25
 - oversampling, X.25
 - serial data, X.23
- CDMA:
 - DSP, signal transmission, X.13
 - military, spread spectrum, X.13
- Cellular telephone, X.11
- Ceramic IC:
 - capacitive effects, XI.18
 - Faraday shield, XI.17
- Charpentier, A., VI.30
- Chebyshev filter, II.39, VII.19
 - comparison with FIR, VII.10
- Circuit noise, XI.36-37
- CISC:
 - architecture, VIII.1-2
 - programming, VIII.1
- Clarke, Robert M., II.51
- CMOS:
 - logic fan-out, XI.53-54
 - noise, XI.57-58
- CMOS DAC, V.3
 - current-steering, V.3
 - voltage-switching, V.3
- CMOS DAC Application Guide, II.51
- CMOS switch, III.37
- CMRR, I.10
- CNI, in receiver, X.16
- Code division multiple access, See: CDMA
- CODEC, speech, X.14
- Coleman, Brendan, III.43
- Colotti, James J., III.43
- Comfort noise insertion, See: CNI
- Common-mode rejection ratio, See: CMRR
- Compact disk, See: CD
- Compact disk player, V.1
 - sigma-delta DAC, VI.22

Complementary bipolar, See: CB
Complex-instruction-set computer, See: CISC
Computation, log and antilog circuits, II.9
Conductor, capacitive noise, XI.16
Continuous grounded conductor, XI.39
Copper foil, XI.3
Cosier, G., X.30
Counts, Lew, II.51
Current feedback amplifier, II.15, 17
Curtin, Mike, X.30

D

DAC, I.2, II.48, III.7, 9, IV.7, VII.1

3-bit,

ideal, digital input, III.20

non-ideal, digital input, III.20

6-bit, V.17

12-bit, architecture, V.15-16

12-bit multiplying, V.16

14-bit,

deglitching, V.14

DSP interface, V.8

functional diagram, V.7

segmentation, V.7

specifications, V.8

16-bit,

glitch impulse, V.10

monotonicity, V.9

MSB, V.9

segmentation, V.8-9

segmented architecture, V.9

specifications, V.10

18-bit, V.6

oversampling, V.6

SNR, V.6

specifications, V.6

18-bit audio, segmentation, V.6

20-bit,

digital offset, V.11

input frequency, V.12

oversampling, V.12

segmentation, V.11

THD+N, V.12

20-bit audio,

digital offset, V.11

input frequency, V.12

segmentation, V.11

THD+N, V.12

architecture, V.1

audio, V.5-6

ac parameters, X.28

clock input, X.28

for, CD, X.28-29

sampling rates, X.28

serial input, X.28

BiMOS, V.4, 8

binary division, V.1

bipolar, V.2

CB processes, V.1-2

CMOS, V.3-4, 7

architecture, V.15-16

FET switches, V.4

construction, V.1-2

current switching, V.1-2

current-steering CMOS, V.3

deglitcher, III.35-36, V.13-14, VI.22

digital filtering, truncation noise, X.28

digital offset, V.10

DNL, III.19

errors, III.19-20

for DSP, V.1

DSP interface, IX.14

DSP parallel interface, IX.27

dynamic performance, III.30-31

dynamic range, III.12

dynamic specifications, III.30

ECL bit switch, V.2

evaluation, V.1

FFT testing, III.34

finite amplitude resolution, III.12

gain errors, III.19

glitch, III.34

glitch impulse, III.33

glitch impulse area, III.32-33

glitch minimization, V.5

glitch reduction, V.10

ground, XI.37

- harmonic distortion, III.33
- high performance applications, V.1
- INL, III.19
- interfacing, IX.1
 - with DSP chip, V.1
- linear, V.17
- minimum glitch, V.5
- MSB, V.11
 - output, IV.1
- multiplying, See: MDAC
- multiplying with digital input, See: LOGDAC
- non-monotonicity, III.19-20
- offset errors, III.19
- output, IV.7
- oversampling ratio, V.1
- parallel, DSP interface, IX.10-11
- PNP differential pairs, V.1
 - as potentiometer, V.15
 - as programmable gain amplifier, V.15
- raster scan display, V.1
- reference voltage, V.15
- resolution and dynamic range, III.12
- sample-and-hold, V.13
- serial, DSP interface, IX.19
- settling time, III.31-32, IV.3
 - refined, III.32
- SHA, V.13
- SHA deglitcher, III.36, V.13
- sin X/X rolloff, III.36
- SNR, V.1
- static performance specifications, III.19
- static transfer characteristics, III.19
- static transfer function, III.19-20
- switching glitch, V.13
- THD, III.35, V.1, 11-12
- track-and-hold, V.13
- TTL bit switches, V.2
- voiceband, V.1
- voltage switches, V.1
- voltage-switching CMOS, V.3-4
- DAC/ADSP-2100, parallel interface, IX.13
- DAC/ADSP-2101:
 - parallel interface, IX.8, 11-12
 - parallel write timing, IX.12
- DAC/TMS32020/C25, parallel interface, IX.13
- DAG, VIII.12-13
 - address pointer, VIII.6
 - addressing, VIII.14
 - features, VIII.13
 - FFT, VIII.12
 - modulus logic, VIII.13
- DAT, ADC, specifications, X.22
- Data acquisition, I.3
 - using ADC, III.29
- Data address generator, See: DAG
- Data bus, high speed, digital noise, XI.20
- Data memory acknowledge, See: DMACK
- Data memory address, See: DMA
- Data memory data, See: DMD
- Data memory select, See: DMS
- Data separator, II.6
- Dattorro, J., VI.30
- Davis, Gary, X.30
- DC converter, II.18
- DCS, IV.6
- DDS, V.1
- Decimation, III.8
- Deglitcher, III.33, V.14
- Del Signore, B.P., VI.30
- Demodulation:
 - analog, III.10
 - direct IF to digital, III.11
- Detector, fast peak, II.4
- DFT, VII.22-24
 - 2-point, FFT decimation, VII.24
 - 8-point, FFT decimation, VII.25
 - butterfly calculation, VII.24
 - equation, VII.23
 - relation to FFT, VII.31
 - signal analysis, VII.24
- DGND, XI.36-38
- Dielectric absorption, capacitor, XI.24
- Differential amplifier, I.10, III.40
- Differential integrator:
 - active, III.41
 - SCF equivalent, III.41

- Differential non-linearity, See: DNL
- Differential receiver input, I.10
- Differentiator, II.2
 - op-amp, II.2
- Digital attenuator, V.18
- Digital audio, I.5, V.1
 - DAC, V.11
- Digital audio oversampling filter, II.49
- Digital audio studio recording, X.20
 - channel processing, X.20
 - D-range distortion, X.22
 - DAT players, X.22
 - DSP signal conversion, X.21
 - FIR filter, X.21
 - mixing, X.20-22
 - multiplier, X.21
 - performance specifications, X.22
 - sampling ADC, X.23
 - sigma-delta audio ADC, X.23
 - SNR, X.22
 - standards, X.22
 - system, X.21
 - techniques, X.21
 - THD+N, X.22
- Digital audio studio system, I.5
- Digital audio tape, See: DAT
- Digital beamforming, II.34
- Digital circuit, noise, XI.36-37
- Digital correction, in subranging ADC, IV.5
- Digital downconversion, III.11
- Digital filtering, VII.1-2
 - ADC, VII.3
 - advantages, VII.2
 - FIR filter, VII.2-3
 - limitations, VII.3
 - and shaped quantization noise, VI.9
 - video, VII.3
- Digital ground, See: DGND
- Digital mobile radio, V.1, X.11
 - CDMA, X.13
 - DSP, X.13
 - TDMA, X.13
- Digital noise, high speed data bus, XI.20
- Digital offset, glitch reduction, V.10
- Digital signal, routing, XI.44
- Digital signal processing, See: DSP
- Digital Signal Processing Applications Using the ADSP-2100 Family, VIII.19
- Digital system, timing variation, XI.54
- Digital voltmeter, IV.8
- Digital-to-analog converter, See: DAC
- Digitally controlled AGC system, V.18
- Digitally corrected subranging, See: DCS
- Diode-connected transistor, II.21, 24
- Direct digital synthesis, See: DDS
- Direct IF to digital demodulation, III.11
- Discontinuous transmission, See: DTX
- Discrete Fourier Transform, See: DFT
- Discrete time sampling, III.1
- Disk drive read, II.5, 7
 - amplifier, II.5-6
- Divider, from multiplier, II.14
- DMA:
 - ADC, IX.4
 - ADSP-2101, IX.4
- DMA bus, ADSP-2101 microcomputer, VIII.7
- DMACK, ADC/ADSP-2101, parallel interface, IX.6
- DMD, ADC, IX.4
- DMD bus:
 - ADSP-2101 microcomputer, VIII.7
 - MAC, VIII.9
- DMS:
 - ADSP-2101, IX.4
 - DSP, IX.1, 8
 - DSP parallel interface, IX.1
- DNL plot, III.25-26
- Doernberg, Joey, III.43
- Downconversion:
 - analog, III.10
 - direct IF to digital, III.11
- DSP56000, serial interface, IX.18, 23
- DSP, I.2, 6, II.34-35, III.8, 33, 37, VII.12, 14-16, 19, 22-23, 30
 - ADC interface, IX.1
 - ADC serial interface, IX.15
 - algorithm, VIII.1-2
 - aliasing, III.9

ALU, VIII.3
 applications, III.16-17
 applications and dynamic range, III.16
 architecture, VIII.2
 bit-reversing, VII.24
 chip select, IX.8
 circular buffer, VII.8, VIII.4
 clock frequencies, IX.26
 code optimization, VIII.1
 CODEC interface, IX.23
 DAC interface, IX.1
 decimation, III.8
 demodulation, III.10
 digital filtering, VII.1
 DMS, IX.1, 8
 dual operand fetch, VIII.3-4
 dynamic analog signal, III.30
 dynamic range, III.16-17
 extended dynamic range, VIII.3
 fast arithmetic, VIII.3
 fast MAC, VIII.3
 FIR filter, VIII.4
 glue logic, IX.1, 16, 27
 hardware, VIII.1
 Harvard architecture, VIII.4
 I/O port interface, IX.23-24
 interfacing, IV.3
 kernel equation, VIII.2
 limitations, VII.1
 MAC, VIII.2
 memory address bus, IX.1
 methods, I.6
 MSB, IX.15
 options, I.6
 oversampling, III.8
 parallel interface, IX.1, 27
 BMS, IX.1
 DMS, IX.1
 IRQ, IX.1
 PMS, IX.1
 writing to DAC, IX.8
 parallel peripheral device write interface,
 IX.9
 processor, VIII.2

RAM, VIII.4
 RD, IX.1
 read process, IX.1
 reading data, IX.1
 RFS, IX.15
 sampled data, III.1
 signal conditioning, III.1
 serial interface, IX.14, 27
 serial port, IX.27
 serial versus parallel interface, IX.26
 in TDMA and CDMA, X.13
 time sampling, analog signals, III.2
 undersampling, III.9
 WR, IX.8
 zero overhead looping, VIII.3
 DSP interface:
 parallel DAC, IX.10
 serial DAC, IX.19
 DSP/ADC, designs, III.21
 DSP/DAC:
 functions, IX.20
 signal requirements, IX.21
 timing relationship, IX.21
 DTX, X.15
 CNI, X.16
 functions, X.16
 SID, X.16
 VAD, X.16

E

E.S.D. Prevention Manual, XI.63
 Eckbauer, F., VI.30
 ECL, noise, XI.58
 Effective aperture delay time, III.27
 Effective number of bits, See: ENOBs
 Eidi, Fares, VII.32
 Einstein, Albert, XI.63
 Electromagnetic force, See: EMF
 Electromagnetic interference, See: EMI
 Electromechanical piezoelectric transducer,
 II.32
 Electrostatic damage, See: ESD
 Elliptical filter, VII.19

- degraded phase response, II.39
 - passband ripple, II.39
 - stopband ripple, II.39
 - EMF, ground loop, XI.35
 - EMI, XI.49-50
 - noise generation, XI.49
 - photoelectric, XI.51
 - in silicon junctions, XI.51
 - prevention, XI.50
 - radiofrequency, XI.49
 - ENCODE command, IV.7
 - Encoder-decoder, II.7
 - Engelhardt, E., VI.30
 - ENOBs, III.12, 21-22, 24
 - ADC, III.15, 21
 - calculation, III.13, 15
 - sinewave curvefit, III.15-16
 - SNR, III.13
 - Error, aliasing, III.40
 - Error correction, Viterbi decoding, X.9
 - ESD:
 - in circuitry, XI.8
 - dust, XI.10
 - low temperature, XI.9
 - protection, XI.8-10
 - Explicit RMS computation, II.19
- F**
- Faraday shield, XI.16-18
 - buffer latch, XI.21
 - Faraday's Laws, XI.2
 - Fast Fourier Transform, See: FFT
 - Fast peak detector, II.4
 - FDM data, III.9
 - FDM signal, III.10
 - super-Nyquist sampling, III.10
 - FDMA, analog cellular radio, X.11-12
 - FDNR, filter configuration, II.41, 43
 - Ferguson, P.F., Jr., VI.30
 - FFT, III.11, 13-14, 33, VII.22-23
 - algorithm, VII.31
 - benchmark processing time, VII.28
 - block floating point, VII.30
 - computational speed, VII.31
 - DAG, VIII.12
 - data scaling, VII.30
 - decimation, DFT, VII.24-25
 - design, VII.27
 - DSP, hardware, VII.27
 - endpoint discontinuities, VII.31
 - as fast implementation of DFT, VII.31
 - hardware, VII.26
 - N-point, computation, VII.26
 - output, ADC, III.14
 - plot, IMD, III.25
 - real-time processing, VII.31
 - real-time speech analysis, VII.27
 - relation to DFT, VII.31
 - resolution, VII.31
 - signal analysis, VII.22
 - sinewave,
 - integral number of cycles, VII.28
 - non-integral number of cycles, VII.29
 - spectral analysis, VII.27, 29
 - spectral leakage, VII.29
 - testing, DAC, III.34
 - windowing, VII.29
 - Filter:
 - active, II.37-38, III.37
 - configurations, II.43
 - active lowpass RC, III.41
 - SCF equivalent, III.41
 - allpass, II.37
 - analog, oversampling, III.9
 - analog lowpass, Nyquist sampling, III.8
 - bandpass, II.37
 - bandstop, II.37
 - Butterworth, II.39
 - capacitance, III.40
 - Chebyshev, II.39
 - class, II.37
 - cutoff frequency, II.38-39
 - design, II.38
 - digital, oversampling, III.9
 - elliptical, II.39
 - FDNR, II.43, 47
 - first-order continuous-time active lowpass,

- III.41
 - highpass, II.37
 - lowpass, II.37
 - conversion to highpass, II.41
 - minimum passband attenuation, II.38-39
 - multiple feedback, II.40-43, 46
 - normalized passive, II.45
 - order, II.38-40
 - parameters, II.38
 - passband ripple, II.38-39
 - passive, II.45
 - normalized values, II.45
 - poles, II.40, III.5, 7
 - programmable state variable, II.48
 - RC, III.41
 - ripple, II.39, 49
 - Sallen-Key configuration, II.40, 43, 46, 50
 - SC, III.40-41
 - sections, II.40
 - seven-pole FDNR 20kHz antialiasing, II.49
 - specifications, II.39-40
 - state variable configuration, II.40-43, 47-48
 - stopband frequency, II.38-39
 - switched capacitor, III.37-40
 - transformation, II.41
 - tuning table, II.44
 - variable bandwidths, III.40
 - wideband Sallen-Key, II.50
- Filtering, II.18
 - digital, See: Digital filtering techniques, III.37
- Finite amplitude resolution:
 - by ADC or DAC, III.12
 - from quantization, III.1
 - LSB, III.12
- Finite impulse filter, See: FIR
- FIR filter, III.8
 - 4-tap, VII.9
 - 69-tap, processor time, VII.15
 - 91-tap, VII.10
 - passband ripple, VII.11-23
 - performance, VII.11
 - audio,
 - CAD design, VII.13-17
 - coefficients, VII.14
 - filter type, VII.14
 - frequency, VII.14
 - gain, VII.14
 - quantization bits, VII.15
 - taps, VII.15
 - audio lowpass, VII.13
 - coefficients, VII.8
 - compared to IIR filter, VII.22
 - data memory addressing, VII.9
 - decimation, VII.19
 - design, VII.6, 8
 - CAD techniques, VII.11-12
 - input, VII.12
 - output, VII.12
 - passband, VII.12
 - stopband attenuation, VII.12
 - theorem, VII.10
 - wordlength, VII.12
 - digital form, VII.3-4
 - direct form, VII.13
 - DSP, VIII.4
 - circular buffering, VII.8
 - equations, VII.8
 - Equiripple FIR design, VII.13
 - filter coefficients, VII.12
 - frequency domain, VII.6-7
 - frequency response, VII.12, 16
 - glitch, VII.22
 - impulse response, VII.7, 10, 12, 17
 - linear phase, VII.18
 - highpass filter, VII.18
 - lowpass filter, VII.18
 - taps, VII.18
 - moving average, VII.4
 - analog signal, VII.5
 - convolution, VII.3, 5
 - sin X/X response, VII.3, 6
 - properties, VII.19
 - step response, VII.17
 - structure, VII.9
 - symmetrical coefficients,
 - highpass filter, VII.18

lowpass filter, VII.18
taps, VII.6, 12
time domain, VII.6-7
transfer function, VII.6
Fisher, J., VI.30
Flash ADC, IV.3-4
 performance, III.22
Flash converter, II.31, 36, IV.5
 for HDTV, IV.4
 sampling ADC, IV.4
FLB, of ADC, III.23-24
Four quadrant multiplier, II.11
Fourier transform, VII.7
 Z-transform generalization, VII.7
FPBW, III.21, 24
 of ADC, III.23
Freeman, D.K., X.30
Frequency dependent negative resistance,
See: FDNR
Frequency division multiple access, See:
FDMA
Frequency division multiplexed, See: FDM
Frequency shift keying, See: FSK
FSK, modulation, X.3
Full wave rectifier, II.4
Full-linear bandwidth, See: FLB
Full-power bandwidth, See: FPBW
Fullscale converter, bit sizes, XI.3
Function generator, for inverse function,
II.14
FWR, II.5-6

G

Galand, C., X.30
Ganesan, A., VI.30
Gaussian minimum shift keying, See: GMSK
General impedance converter, See: GIC
General switched telephone network, See:
GSTN
Ghausi, M.S., II.52, III.44
GIC, filter configuration, II.41, 43
Gilbert, Barrie, II.51
Gilbert Cell, II.10-11

Glitch energy, III.32
Glitch impulse, III.33-34
 area, III.32-33
Glitch reduction:
 by segmentation, V.5
 techniques, V.15
GMSK:
 I/Q RF demodulator, X.19
 spectral leakage minimizing, X.18
Gold, Bernard, III.44, VII.32
Gray, G.A., III.43
Ground, current noise, XI.34
Ground loop, XI.34-35
 and EMF, XI.35
Ground noise, XI.34
Ground plane, XI.40
 breaks, inductance, XI.41
 mixed signal system, XI.44
 in PCB, XI.39
 residual resistance, XI.39
Grounding, XI.32
 ideal, XI.33
 realistic, XI.33
GSM, X.11, 13-14
 baseband I/O port, X.18-20
 specifications, X.20
 cylinders, X.15
DAC, GMSK-coded ROM, X.19
discontinuous transmission, X.14
downconversion, X.18
DTX, X.15
equalization, X.14
FIR filter, X.18-19
frequency-time allocations, X.19
modulation, GMSK, X.18
modulation/demodulation, X.14
sigma-delta ADC, X.18-19
speech compression, X.15
speech encoder and decoder, X.14
TDMA, X.18
transcoder, X.14
upconversion, X.18
Viterbi decoder, X.14
GSTN, V.32 modem, X.4

Guard ring, insulation resistance, XI.7

H

Hanning window, VII.29-30
 Harmonic distortion, III.21, 33
 and ADC performance, III.17
 Harris, Frederic J., III.43, VII.32
 Harris, Steven, VI.30
 Harvard architecture, DSP, VIII.4
 Haspeslagh, J., X.30
 HDTV, I.3
 flash converter, IV.4
 Heise, B., VI.30
 Hellwig, K., X.30
 Higgins, Richard J., I.18, III.44, VII.32
 High frequency decoupling, analog circuit, XI.23
 High frequency instability, analog circuit, XI.24
 High performance analog circuit, prototyping, XI.61
 High speed cable driving, configurations, I.16
 High Speed Design Seminar (1990), I.18, II.51, III.44, V.19, VII.32
 High-definition television, See: HDTV
 High-gain limiting amplifier, II.15-16
 Higher order modulator loop:
 dynamic range, VI.12
 idling pattern, VI.12
 stability, VI.12
 Hodges, David A., III.43-44
 Hofmann, R., X.30
 HP Journal, III.43
 HP Product Note, III.43
 Huelsman, L.P., II.52
 Hughes, Richard Smith, II.51

I

ICNTL, VIII.14
 IEEE Trial-Use Standard for Digitizing Waveform Recorders, III.44
 IFC, VIII.14
 IIR filter, VII.19

analog counterpart, VII.19
 biquad, VII.19
 compared to FIR filter, VII.22
 digital, VII.19
 efficiency, VII.21
 feedback, VII.21
 first-order, lowpass, VII.20
 general equation, VII.19, 21
 glitch, VII.22
 minimum sampling period, VII.21
 non-linear phase, VII.21
 properties, VII.21
 second order, VII.19
 second-order, lowpass, VII.20
 throughput, VII.21
 IMASK, VIII.14
 IMD, III.25
 FFT plot, III.25
 Implicit RMS computation, II.20
 Inductance:
 ground plane breaks, XI.41
 mutual, XI.26
 signal routing, XI.26
 stray, XI.25
 wire, XI.25
 Inductive coupling:
 principles, XI.27
 ringing, XI.29
 Inductor:
 parasitic effects, XI.30
 Q, XI.32
 saturation, XI.30-31
 Industrial process control, sigma-delta ADC, VI.16, 19
 Infinite impulse response, See: IIR
 INL:
 ADC, III.17
 DAC, III.19
 Input signal, oversampling, III.8
 Instrumentation amp, I.10-11
 3 op-amp, I.11
 adder, II.1
 common mode voltage, I.11
 high performance, I.12

high performance-high speed, I.12
high speed, I.12-13
 pulse response and settling time, I.13
pulse response, I.13
settling time, I.13
subtractor, II.2
wideband, I.12-13
Insulator, leakage, XI.6
Integral non-linearity, See: INL
Integrated circuit, III.37, 39
 ESD, XI.9
Integrated circuit log amp, II.28-29
 cascaded, II.30
 dc coupling, II.29
 features, II.29
 laser-trimmed, II.28
 transfer function, II.29
Integrator, op-amp, II.3
Intercept voltage, II.20
Intermodulation distortion, See: IMD
International EMI Emission Regulations,
 XI.63
International Telegraph and Telephone Con-
 sultative Committee, See: CCITT
Interrupt control register, See: ICNTL
Interrupt force and clear, See: IFC
Interrupt mask register, See: IMASK
Inverting adder, II.1
Inverting op-amp, II.21, 23
IRQ, DSP parallel interface, IX.1
Isolation amplifier, I.17
 three-port, I.17

J

Johnson noise, resistor, XI.14-15
Jones, Ralph, X.30

K

Karagozyan, Kapriel, IX.28
Kaufman, Sid, III.43
Kelvin feedback, XI.6
Kester, W.A., III.44
Kirchoff's Law, XI.2, 26, 32

Kitchin, Charles, II.51
Koch, R., VI.30

L

Laker, K.R., II.52, III.44
Laplace transform, VII.7
Laser trimming of resistor, II.11
Leakage, insulator, XI.6
Leakage resistance, PCB, XI.7
Least significant bit, See: LSB
Lee, Hae-Seung, III.43
Lee, Wai Laing, VI.30
Lenz's Law, XI.2
Line driver, balanced, I.13-15
Linear coded ADC and DAC, VI.25
Linear predictive coding, See: LPC
Log amp, II.9, 20-24, 28, 31-32
 basic, II.22
 broadband operation, II.30
 cascaded, II.30-32
 detector, II.22, 27
 diode/op-amp, II.23
 disadvantages, II.10
 error curve, II.29
 with flash converter, II.31
 full-wave detector, II.21
 gain, II.26
 intercept voltage, II.20
 key parameters, II.27
 logarithmic transfer, II.29
 multi-stage, II.25-26
 specifications, II.26-27
 successive detection, II.27-28
 transfer, II.21
 transistor, II.24
 true, II.23, 32
Log strip, II.28
Log video amp, II.23, 31-32
Logarithmic amplifier, See: Log amp
Logarithmic converter, II.20
LOGDAC, I.6, V.17
 8-bit, V.18
 applications, V.18

LSB, V.17
 ROM decoder, V.17
 Logic:
 fan-out, limitations, XI.52-53
 mixed signal systems, XI.52
 noise, XI.57-58
 sampling clock noise, XI.55-56
 timing,
 temperature variation, XI.55
 variation, XI.54
 Low frequency measurements, sigma-delta
 ADC, VI.16, 19
 LPC, cylinders, X.15
 LPC algorithm, X.14
 LSB, II.31, III.12
 in comparator, IV.3
 size, fullscale converter, XI.3

M

MAC, VIII.9-10
 DMD bus, VIII.9
 features, VIII.10
 instructions, VIII.11
 PMD bus, VIII.9
 register, VIII.9
 Magnetic field, shielding, XI.28-29
 Mahoney, Matthew, III.44
 Mar, Amy, VII.32
 MASH:
 cascaded stable first-order loops, VI.26
 digital differentiator, VI.27
 modulator, VI.27
 sigma-delta ADC, VI.26
 topology, VI.27
 Matsuya, Y., VI.30
 Maximally flat filter, II.39
 MDAC, V.15
 4-quadrant, V.16
 configuration, V.16
 12-bit, features, V.17
 16-bit linear,
 attenuation, V.17
 selected inpput codes, V.17
 applications, V.18
 bipolar input, V.15
 construction, V.16
 Mecca ground, XI.36
 MECL System Design Handbook, XI.63
 Meehan, Pat, III.43
 Memory read, See: RD
 Metal lids, on ceramic IC package, XI.18
 Microcomputer, ADSP-2101, VIII.5
 Microstrip:
 controlled impedance, mixed signal system,
 XI.44
 transmission line, XI.41
 Minimum 4-Term Blackman-Harris window,
 VII.29, 31
 Mixed signal circuit, XI.1
 design, XI.2
 prototyping, XI.61
 Mixed signal processing, I.1-2, X.1
 definition, I.5
 Mixed signal system:
 ground plane, XI.44
 signal routing, XI.44
 Mode status register, See: MSTAT
 Modem, V.1, X.1-3
 CCITT recommendations, X.3
 demodulation, X.1
 echo cancellation, X.1
 error detection and correction, X.1
 full-duplex, X.2
 half-duplex, X.2
 hybrid circuit, X.2
 modulation, X.1
 modulation methods, X.3
 V.32,
 adaptive equalizer, X.7-8
 ADC, X.5, 7-10
 analog front end, X.9-10
 antialiasing filter, X.8, 10
 characteristics, X.4
 CODEC, X.10
 DAC, X.5-6, 9
 demodulator, X.7-8
 descrambler, X.7-8

diagram, X.5
differential decoder, X.7-8
echo canceller, X.7-8
error correction, X.9
filter chips, X.10
FIR filter, X.9
GSTN, X.4
I/O port, X.8, 10
input antialiasing receiver, X.7-8
modulation, X.5-6
pulse shaping filter, X.7
QAM, X.5
receiver, X.7-8
SCF, X.10
signal constellation, X.6
signal separation, X.8
SNR, X.10
THD, X.10
transmitter, X.5-6
Viterbi decoder, X.7-9
Modulation:
 ASK, X.3
 FSK, X.3
 PSK, X.3
 QAM, X.3
Modulator, II.15-6
 as precision rectifier, II.16
Momentum Data Systems, Inc., VII.32
Morley, Nick, X.30
MSB, III.33
MSTAT, VIII.14
Multi-bit sigma-delta converters, VI.27
Multi-stage noise shaping, See: MASH
Multiple feedback, filter configuration, II.40-43
Multiplier:
 2-quadrant linear, II.11
 4-quadrant, II.15
 translinear, II.12
 as audio power meter, II.13
 basic, II.8
 basic transconductance, II.10
 direct divide capable, II.15
 as divider, II.14

 Gilbert cell, II.11
 in op-amp, II.14
 as power meter, II.13
 signal output, II.15
 trimmable error, II.12
 types, II.9
 VGA, II.17
Multiplier-accumulator, See: MAC
Multiplying DAC, See: MDAC
Murphy's Law, XI.1
 corollary, XI.2

N

N-Bit flash converter, IV.3
Nahman, Norris S., III.43
Net midscale glitch, III.33-34
Non-inverting adder, II.2
NRZ data, II.5, 7
Nyquist bandwidth, III.8-9, 12-13, 23-24
Nyquist criterion, III.2-3, 7, 9
Nyquist limit, III.35, 42
Nyquist sampling, analog lowpass filter, III.8, VI.2
Nyquist theorem, III.37

O

Ohm's Law, XI.2
Ohm's law, PCB copper foil, XI.4
Op-amp, I.7, III.37, IV.4, V.4
 absolute value circuit, II.4
 adder, II.1
 basic configuration, I.9
 configuration, I.8-9
 differentiator, II.2
 dynamics, II.48, IV.4
 external, for buffered output voltage, II.31
 filters, II.37
 high-performance, II.1
 ideal equations, I.9
 instrumentation, I.10-11
 integrator, II.3
 inverting, I.9
 level shifter, I.9

- ideal equations, I.9
- non-inverting, I.9
- performance, III.22
- specifications, I.8
- subtractor, II.2
- Operational amplifier, See: Op-amp
- Oppenheim, A.V., VII.32
- Oscillator:
 - Colpitts, XI.57
 - noise, XI.57
- Oversampling:
 - analog filter, III.9, VI.3
 - digital filter, III.9, VI.3
 - ratio, III.8-9
- Overvoltage recovery time, III.30

P

- PAL color subcarrier frequency, I.15
- Pan-European Digital Cellular Radio System (Groupe Speciale Mobile), See: GSM
- Parallel DAC, DSP interface, IX.10
- Parallel peripheral device, read interface, IX.3
- Parks-McClellan algorithm, VII.12
- Parzefall, F., VI.30
- Passive RC network, SC equivalent, III.39
- PC track, transmission line, XI.40
- PCB:
 - capacitance, XI.15-16
 - differential transmission, XI.46
 - edge connections, XI.45
 - flowchart layout, XI.45
 - ground error minimization, XI.46
 - as ground plane, XI.39
 - grounding, XI.42
 - guard ring, XI.7
 - multiple card system,
 - ground, XI.43
 - star analog ground, XI.43
 - multiple ground pins, XI.46
 - prototyping, XI.61-62
 - SPICE modeling, XI.59

- Teflon stand-off insulator, XI.7-8
- thermoelectric effects, XI.12
- transmission line, XI.40
- PCB copper foil, XI.3
 - anisotropy, XI.6
 - insulation, XI.6
 - Ohm's law, XI.4
 - skin effect, XI.4-5
 - track resistance, XI.4
- Peak detector, II.4-6
- Peak harmonic content, III.23
- Peak spurious component, III.23
- Peak spurious response, III.23
- Phase shift keying, See: PSK
- Phase-locked loop, in disk drive read amplifier, II.6-7
- Phased array, digital, II.34
- Phased array ultrasound, II.34
- Physics, laws, XI.2
- PMA bus, ADSP-2101 microcomputer, VIII.7
- PMD bus:
 - ADSP-2101 microcomputer, VIII.7
 - MAC, VIII.9
- PMS, DSP parallel interface, IX.1
- Pohlmann, Ken, X.30
- Polarity, in analog multiplier, II.8
- Pole, filter, II.40
- Potentiometer, V.15
- Power supply:
 - for electronic circuit, XI.47
 - noise, XI.47-48
 - switching-mode, XI.48-49
 - noise, XI.48
- Precision analog circuit, ESD, XI.9
- Precision rectifier, II.15-16
- Pressure measurement, sigma-delta ADC, VI.16, 19
- Printed circuit board, See: PCB
- Process control, I.3
- Processor interrupt request, See: IRQ
- Program memory address, See: PMA
- Program memory data, See: PMD
- Program memory select, See: PMS
- Program sequencer, VIII.14

ADSP-2101 microcomputer, VIII.15

ASTAT, VIII.15

features, VIII.15

ICNTL, VIII.15

IFC, VIII.15

IMASK, VIII.15

MSTAT, VIII.15

SSTAT, VIII.15

Programmable gain amplifier, V.15, 18

Programmable Lowpass Analog Filter Using
12-Bit DACs, II.51

Programmable power supply, V.18

Programmable state variable filter, II.48

Prototyping, XI.61-62

PSK, modulation, X.3

Public Switched Telephone Network, See:
GSTN

Q

Q:

inductor, XI.32

resonant circuit, XI.32

QAM, DAC, X.7

Quadrature amplitude modulation, See:

QAM

Quality factor, See: Q

Quantization, III.12-13

Quartz crystal, Q, XI.32

R

Rabiner, Lawrence R., III.44, VII.32

Radix-2 decimation-in-time, FFT butterfly,
VII.26

Radix-2 FFT, VII.24-26

benchmark processing time, VII.28

Radix-4 FFT, VII.24-25

algorithm, VII.26

benchmark processing time, VII.28

RAM, fixed boundary, VIII.4

RAMDAC, I.4

Ramirez, Robert W., III.43, VII.32

RC filter:

SCF equivalent, III.37, 39

single-pole passive, III.37, 39

RD:

ADSP-2101, IX.4

DSP, IX.1

RD timing, ADSP-2101, IX.2

Real-world signal, processing, I.3

Receive frame synchronization, See: RFS

Receiver, balanced, I.13-15

Rectifier, full wave, II.4

Recursive subranging, IV.7

Reduced-instruction-set computer, See: RISC

Reidy, John, III.43, X.30

Remez exchange algorithm, VII.12

Resistance, conductor, XI.3

Resistive system, logic fan-out, XI.53-54

Resistor:

equivalent circuit, XI.11

inductance, XI.11

Johnson noise, XI.14-15

mismatch, XI.13

parasitic effects, XI.11

induction, XI.11

thermal noise, XI.14

thermal stability, XI.13

thermoelectric effects, XI.12

voltage variation, XI.13-14

wirewound, thermocouple, XI.12

Resonant circuits, from decoupled power
lines, XI.30

RFS, DSP, IX.15

Ribbon cable:

mutual inductance, XI.28

signal coupling, XI.28

Ringling, XI.29

RISC:

application, VIII.1

architecture, VIII.1-2

DSP, VIII.1

programming, VIII.1

RMS, II.18

RMS conversion:

explicit, II.19

implicit, II.20

wideband, II.19

RMS quantization, III.13
 noise, III.13
 RMS value:
 explicit method, II.18-19
 implicit method, II.18, 20
 Root mean square, See: RMS
 Rosso, M., X.30

S
 S/N+D, III.21-22
 Sallaerts, D., X.30
 Sallen-Key filter, II.40, 43, 50
 frequency response, II.50
 Sample-and-hold amplifier, See: SHA
 Sampled data system, III.1
 Sampling clock, design, noise minimization, XI.56
 SAR, IV.1
 ADC encoder, IV.3
 ADC with SHA, IV.2
 clock-to-data-output delay, IV.3
 input data setup time, IV.3
 SAW, III.37
 SCF, III.37, 40
 bandwidth, III.38
 sampling device, III.37
 Schafer, R.W., VII.32
 Schoenwetter, Howard K., III.43
 Serial port:
 features, VIII.17
 interface lines, VIII.16
 Settling time, III.29, 31-32
 Seven-pole FDNR 20kHz antialiasing filter, II.49
 SFDR, III.23
 SHA, II.5-6, III.21-22, 24, IV.1, 3-4, 7
 degitcher, III.35-36, V.13-15
 switching transients, V.13
 SHA-ADC pair, III.21
 Shaped quantization noise, and digital filtering, VI.9
 Sheingold, Daniel H., I.18, II.51, III.43, V.19
 Shifter, VIII.11

 features, VIII.12
 instructions, VIII.12
 operations, VIII.12
 SID, in receiver, X.16
 Sigma-delta ADC, VI.1
 16-bit, VI.16-17
 calibration, VI.17
 digital filter response, VI.18
 digital filter step response, VI.18
 mixed signal device, VI.24-25
 modulator, VI.17
 18-bit audio, VI.13
 amplitude response, VI.15
 antialiasing filter, VI.13
 digital filter, VI.15
 modulator output, VI.14
 specifications, VI.14
 21-bit,
 digital filter response, VI.20
 features, VI.19-20
 high-level analog input, VI.21
 on-chip signal conditioning, VI.19
 single-channel differential low-level PGA input, VI.21
 two-channel differential low-level PGA input, VI.21
 22-bit,
 configuration, VI.19
 low frequency measurement, VI.19
 DAC, VI.3, 27
 decimation, VI.1, 8-10
 digital filtering, VI.1, 8-10, 16
 filter output, VI.8
 FIR filter, VI.8, 10
 first-order, VI.4
 noise shaping, VI.6-7
 first-order modulator,
 idling pattern, VI.11
 integrator output, VI.11
 higher order modulator loops, VI.12
 idling pattern, VI.11
 IIR filter, VI.8, 10
 low frequency measurements, VI.16, 19
 MASH, VI.26

- for mixed signal VLSI, VI.1
- modulator, VI.3-4
 - bit pattern, VI.11
 - frequency domain model, VI.5
 - second-order, VI.6-7
 - waveforms, VI.4
- multi-bit, first-order, VI.27
- noise-spectrum shaping, VI.1-2
- Nyquist sampling, VI.2
- oversampling, VI.1-3, 8, VII.19
- quantization noise shaping, VI.3
- second-order, VI.6-7
 - noise shaping, VI.6-7
- second-order modulator,
 - idling pattern, VI.12
 - second integrator output, VI.12
- shaped quantization noise, VI.9
- shaped quantization noise distribution, VI.6
 - SNR, VI.6, 8
 - synchronous voltage-to-frequency converter, VI.5
 - tonal considerations, VI.11
 - two-stage filter, VI.10
- Sigma-delta architecture, IX.27
- Sigma-delta CODEC:
 - decoder, VI.25-26
 - linear coded ADC and DAC, VI.25
 - mixed signal device, VI.24-25
- Sigma-delta converter, III.7
 - limits, VI.28
 - MASH, VI.26
 - multi-bit, VI.27
 - multi-bit versus single bit, VI.28
 - oversampling, III.7
 - summary, VI.29
- Sigma-delta DAC:
 - 16-bit,
 - analog filter, VI.23
 - digital modulator, VI.23
 - discrete time signal, VI.24
 - IIR filter, VI.23
 - mixed-signal device, VI.24-25
 - shaped quantization noise, VI.23
 - voiceband output, VI.23
 - antialiasing filter, VI.21
 - in compact disk players, VI.22
 - concepts, VI.22
 - deglitcher, VI.23
 - glitches, VI.22
 - lowpass filter, VI.22
 - mixed-signal IC architecture, VI.21
 - noise filtering, VI.21
 - oversampling, VI.21
- Signal:
 - ADC, I.2
 - analog, I.1
 - attenuation, II.32
 - autocorrelation, I.3
 - characteristics, I.1
 - conditioning, I.1, 8
 - op-amp, I.7
 - convolution, I.3
 - definition, I.1
 - digital, I.1
 - dynamic range, for ADC selection, III.16
 - filtering, I.3
 - magnitude, II.18
 - origin, I.1
 - output, of multiplier, II.15
 - processing, I.2
 - analog, See: Analog signal processing
 - analog vs. digital, I.5-7
 - frequency content compression, I.2-3
 - real-time, I.5
 - real-world, I.2
 - ASP, I.4
 - digitally synthesized, I.4
 - DSP, I.4
 - generation, I.4
 - MSP, I.4
 - processing, I.3-4
 - TDM, I.2
- Signal lead, voltage drop, XI.6
- Signal routing, XI.32, 44
 - mutual inductance, XI.26-27
- Signal voltage:
 - Mecca ground, XI.36

ground, XI.36
 signal-to-noise plus distortion, See: S/N+D
 signal-to-noise ratio, See: SNR
 source descriptor, See: SID
 silicon junction transistor, transconductance, III.10
 sinewave curvefit, for ENOBs, III.15
 $\sin(x)/x$ frequency rolloff effect, III.35-36
 Skin effect:
 DC circuit, XI.4
 PC board dielectric, XI.5
 PCB copper foil, XI.4-5
 Slattery, Bill, XI.63
 Slope voltage, II.21
 Sluyter, R.J., X.30
 SNR, III.12, 21, 24, 27, 33
 calculation, III.13-15
 ENOBs, III.13
 measurement, III.21-22
 Socket:
 capacitance, XI.60
 high performance analog circuit, XI.60
 inductance, XI.60
 resistance, XI.60
 undesirable in circuit, XI.60
 Sodini, C.G., VI.30
 Soft-body tissue attenuation, II.32
 Southcott, C.B., X.30
 Spectral analysis, VII.23
 Speech CODEC, X.14
 SPICE, modeling, limitation, XI.58-59
 Spurious free dynamic range, See: SFDR
 SSTAT, VIII.14
 Stack status register, See: SSTAT
 Star ground, XI.36
 State variable, filter configuration, II.40-43
 Stray capacitance, chip bondwires, XI.19
 Subtractor, II.3
 instrumentation amp, II.2
 op-amp, II.2
 Successive approximation architecture, IX.27
 Successive detection log amp, II.21
 Summing amplifier, II.26
 Super-Nyquist, III.9, 11

sampling, FDM signal, III.10
 Swanson, E.J., VI.30
 Switched capacitor:
 CMOS, III.39
 resistor, III.38
 Switched capacitor filter, III.37
 advantages, III.40
 limitation and error source, III.42
 as resistor, III.37, 39-40
 Switched capacitor integrator, III.41
 System ground, XI.42
 System interface, ADSP-2101 microcomputer, VIII.17

T

T-Carrier, digital voice transmission, X.14
 Tant, M.J., III.44
 TDM signal, I.2
 TDMA, DSP, signal transmission, X.13
 Telephone:
 diagram, X.2
 imperfections, X.1
 long distance transmission, X.2
 Television transmultiplexer, III.9
 Temperature measurement, sigma-delta ADC, VI.16, 19
 TGA, II.32-34, 36
 THD+N, for 20-bit audio DAC, V.12
 THD, III.21, 23, 33-35
 Thermometer code, IV.4
 Time division multiple access, See: TDMA
 Time division multiplexed, See: TDM
 Time gain amplifier, See: TGA
 TMS32020/C25, serial interface, IX.19, 22
 Total harmonic distortion, See: THD
 Track-and-hold, for deglitching, V.13
 Transcoder, X.14
 Transducer, slow, IV.8
 Transient response, III.29
 Transimpedance amplifier, II.15
 Translinear multiplier, II.11, 13, 15-16
 Transmission line, XI.40
 Transmit data, See: DT

True log amp, II.21, 31

TTL:

- logic fan-out, XI.53-54

- noise, XI.57-58

Tukey, J.W., III.43

Tuned circuit, XI.29

- from stray capacitance, XI.31

U

Ultrasound, II.32-33

- amplifier, II.34-35

- phased array, II.34

- VGA, II.36

Undersampling, III.9

V

VAD, DTX, X.16

Van Valkenburg, M.E., II.51

Variable gain amplifier, See: VGA

Vary, P., X.30

Very large scale integration, See: VLSI

VGA, II.5-6, 15, 17-18, 32-33, 35-6

- AC response, II.18

- independent gating, II.36

- multiplier, II.17

- single channel, II.36

- transient response, II.18

Video amp, II.21, 23

Video line driver, low differential gain and phase, I.16

Video signal transmission, transmission, XI.47

Viterbi decoding, X.9

VLSI, I.5, IV.3, 9

Voice activity detection, See: VAD

Voice encoding, CODEC, X.14

Voiceband filter, III.38

Voltage:

- RMS value, II.18

- See also EMF

Voltage drop:

- resistive, gain error, XI.6

- sense connection, XI.6

Voltage-controlled attenuator, II.36

W

Wainwright Instruments GmbH, XI.63

Wainwright Instruments Inc., XI.63

Weeks, Pat, III.43

Weigh scales, sigma-delta ADC, VI.16, 19

Weighting function, VII.31

Welland, D.R., VI.30

Wideband amplifier, I.12

- variable gain low noise, II.35

Wideband RMS measurement, II.19

Wideband Sallen-Key filter, II.50

Williams, A.B., II.51

Williams, C.S., VII.32

Wooley, Bruce, VI.30

WR, DSP, IX.8

Write output, See: WR

Wynne, John, XI.63

Z

Zeoli, G.W., III.43

Zverev, A.I., II.51

MIXED SIGNAL PROCESSING DESIGN SEMINAR

ADSP-2111, VI.25
ADSP-21msp50, X.14, 16-18
ADSP-21msp01, X.10-11
ADSP-28msp02, VI.24-25, IX.1, 23, 25-6,
X.10

S

SSM-2141, I.14-15
SSM-2142, I.14-15

ANALOG DEVICES PART INDEX

INDEX

A
AD210, I.17
AD521, I.10
AD522, I.10
AD534, II.11
AD538, II.21, 24
AD539, II.15, 17
AD545
AD56
AD5
AD7
AD
AD
A
/

AD1865, X.25-27
AD1876, X.23
AD1879, VI.1, 12-15, 26-28, X.23
AD7002, X.18-20
AD7111, V.17-18
AD7341, X.9-10
AD7371, X.9-10
AD7528, II.48, 51
AD7701, VI.16-18
AD7703, VI.17, 19
AD7710, VI.19-21
AD7711, VI.19-21
AD7712, VI.19-21
VI.6-8, IX.10-13

INDEX-24